ABSTRACT

In a data log acquisition circuit 100, the number of executed test patterns counted by a number-of-patterns counter 1, or the address of the test pattern is compared with a predetermined reference value by an identity detection circuit 2. If the number of executed test patterns or the address of the test pattern and the predetermined reference value are data for the same test pattern, an identity signal is supplied to a log mode control circuit 3. The address of the test pattern is written into a log memory 6 at timing adjusted by a timing adjustment circuit 4 correspondingly to a write address of a data log generated by a counter 5 in accordance with an established operation mode. The write address and the address of the test pattern are held temporarily by a flip-flop 9. The number of generated FAIL signals is counted and outputted by a counter 10.